Exhibit 1

UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

SOLAS OLED LTD., *Plaintiff,* v. DELL INC., *Defendant.*	Case No. 6:19-cv-00514-ADA
SOLAS OLED LTD., *Plaintiff,* v. GOOGLE LLC, *Defendant.*	Case No. 6:19-cv-00515-ADA
SOLAS OLED LTD., *Plaintiff,* v. APPLE INC., *Defendant.*	Case No. 6:19-cv-00537-ADA
SOLAS OLED LTD., *Plaintiff,* v. HP INC., *Defendant*	Case No. 6:19-cv-00631-ADA

DECLARATION OF RICHARD A. FLASCK IN SUPPORT OF SOLAS'S OPENING CLAIM CONSTRUCTION BRIEF

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TABLE OF EXHIBITS AND ABBREVIATIONS

Ex[1]	Document Description	Abbreviation
2	U.S. Patent No. 6,072,450	'450 patent
3	U.S. Patent No. 7,447,338	'338 patent
4	U.S. Patent No. 7,573,068	'068 patent
5	U.S. Patent No. 7,499,042	'042 patent
6	U.S. Patent No. 7,663,615	'615 patent
7	Parties' joint revised list of terms/constructions dated June 12, 2020	Joint Chart
8	The Authoritative Dictionary of IEEE Standards Terms (7th ed. 2000) ("IEEE Dictionary"), definitions of "drain," "source," select," and "substrate"	IEEE Dict.
9	Microsoft Computer Dictionary (3rd ed., 1997), definition of "signal" and 'scan line"	MS Dict.
10	McGraw-Hill Dictionary of Scientific and Technical Terms (4th ed., 1989), definitions of "data transmission line," "source," drain," and "selection circuit"	McGraw-Hill
11	Merriam-Webster Dictionary (avail. at www.merriam-webster.com, accessed May 2020), definitions of "select," "selection," "sequential," and "series."	Merriam-Webster
12	Dictionary.com (avail. at www.dictionary.com, accessed May 2020), definitions of "period," "section," "sequence," and "sequential"	Dictionary.com
13	Oxford Concise Dictionary (12th ed., 2011), definitions of "period" and "section"	Oxford Concise
14	Claim Construction Memorandum and Order from *Solas OLED Ltd. v. Samsung Display Co., Ltd.*, 2:19-CV-00152-JRG, Dkt. 99 (E.D. Tex. Apr. 17, 2020)	Samsung Markman
15	Claim Construction Order from *Solas OLED Ltd. v. LG Display Co., LG Elec., Inc., and Sony Corp.*, Dkt. 82, Case 6:19-cv-00236-ADA (W.D. Tex. June 9, 2020)	LG/Sony Markman
16	Parties' Joint Claim Construction Statement from *Solas OLED Ltd. v. LG Display Co., LG Elec., Inc., and Sony Corp.*, Dkt. 76, Case 6:19-cv-00236-ADA (W.D. Tex. May 1, 2020)	LG/Sony JCC

[1] All exhibits attached to the concurrently filed declaration of Philip X., Wang

I, Richard A. Flasck, declare and state as follows:

I. INTRODUCTION

1. I have been retained as an expert in the above-captioned cases by Solas OLED Ltd. ("Solas"). I understand that Solas has asserted five patents in these cases: U.S. Patent Nos. 6,072,450 ("'450 patent"), 7,446,338 ("'338 patent"), 7,573,068 ("'068 patent"), 7,499,042 ("'042 patent"), and 7,663,615 ("'615 patent") (collectively "Asserted Patents").

2. I have been asked to consider and opine on claim constructions for disputed claims terms in these patents, which I set forth and address in separate sections below for each term.

3. In forming my opinions, I have reviewed, considered, and/or had access to the patent specifications and claims, their prosecution histories, the parties' proposed claim constructions, and the extrinsic evidence cited by the parties in connection with those proposed constructions. I have also relied on my professional and academic experience in the fields of flat panel, active-matrix, and/or LED displays. I reserve the right to consider additional materials as I become aware of them and to revise my opinions accordingly.

II. QUALIFICATIONS

4. My qualifications for forming the opinions set forth in this Declaration are summarized here and explained in more detail in my *curriculum vitae*, which is attached as Exhibit A.

5. I received a Bachelor of Science degree in Physics from the University of Michigan, Ann Arbor, in 1970. I thereafter received a Master of Science degree in Physics from Oakland University in Rochester, Michigan, in 1976. I am the founder and CEO of RAF Electronics Corp., where I developed and patented Liquid Crystal on Silicon (LCOS) microdisplay projection technology using active matrix transistor arrays as well as developed proprietary LED-based Solid State Lighting (SSL) products.

6. After receiving my bachelor's degree, I was employed as a scientist and a manager by Energy Conversion Devices, Inc., from 1970 through 1982. My work at Energy Conversion Devices concerned the development of electroluminescent displays, thin film photovoltaics, ablative imaging films, non-volatile memory, multi-chip modules, and superconducting materials. After leaving Energy Conversion Devices, I founded and served as CEO of Alphasil, Inc., where I developed amorphous silicon thin film transistor (TFT) active matrix liquid crystal displays (AMLCDs). My work at Alphasil included thin film transistor array substrate process and circuit design, data driver and gate driver design, scalers, video circuits, gamma correction circuits, backlighting, and inverter design. At Alphasil I also designed and incorporated touch panel screens into active matrix display devices. The touch panel technologies included surface acoustic wave and capacitive sensing. I worked at Alphasil from 1982 through 1989.

7. After leaving Alphasil, I founded RAF Electronics Corp., described above. I have served as CEO of RAF Electronics since that time. At RAF I developed HDTV projection technology including transistor array substrates for LCOS devices and the associated optical systems. My activities at RAF have included developments in lighting systems using both traditional LED and OLED (Organic Light Emitting Diode) technologies. In 2016 I was granted US Patent 9,328,898 which includes OLED and LED technology and lighting systems. In 2019 RAF received a CalSEED grant from the California Energy Commission to develop ultra-efficient lighting products and explore establishing a Central Valley manufacturing facility.

8. In 1997, I took the position of President and COO at Alien Technology Corporation, where I was responsible for completing a Defense Advanced Research Projects Agency (DARPA) contract, and for implementing MEM fluidic self-assembly (FSA) technology. I left that position in 1999.

9. In 2002, I co-founded and served as COO of Diablo Optics, Inc., where I developed, produced, and commercialized key optical components for HDTV projectors, such as polarization optics, condenser lenses, projection lenses, and ultra-high performance optical interference filters using thin film stacks in conjunction with LED and thin film transistor arrays and devices. I left Diablo in 2007.

10. I am listed as an inventor on twenty-six patents issued in the United States and foreign countries, including one United States design patent. My inventions concern technologies including LED devices, semiconductor materials, glass materials, non-volatile memory cells, thin film transistors, flat panel backplanes and displays, and wafer based active matrices, and various transistor array substrates.

11. I have authored or co-authored twenty-five articles or conference presentations, including numerous papers and presentations concerning lighting and display technologies. My curriculum vitae (Exhibit A) lists these articles, conference presentations, and patents.

12. I am also a member of several professional organizations, including the OSA, SPIE, AES, SID, and the IEEE.

13. In summary, I have almost 50 years of experience in the field of high tech product development including flat panel displays, transistor array substrates, touch panels, and OLED and LED devices.

14. In the past twelve years, I have served as an expert witness for patent infringement litigation (or arbitrations) or PTAB proceedings in the following cases:

- *Nichia Corporation v. Seoul Semiconductor*, 3:06-cv-0162 (NDCA), on behalf of Seoul Semiconductor Company, Inc.

- *Hewlett Packard v. Acer Incorporated et al.*, U. S. ITC Investigation No. 337-TA-606, on behalf of Acer Incorporated et al.
- *Samsung v. Sharp*, U. S. ITC Investigation No. 337-TA-631, on behalf of Samsung
- *Sharp v. Samsung*, U. S. ITC Investigation No. 337-TA-634, on behalf of Samsung
- *O2Micro v. Monolithic Power Systems et al.*, U. S. ITC Investigation No. 337-TA-666, on behalf of O2Micro
- IPR No. IPR2014-0168 of U.S. 7,612,843, on behalf of Petitioner Sony, Corp.
- *Ushijima v. Samsung*, 1:12-cv-00318-LY (WDTX), on behalf of Ushijima
- *Delaware Display Group LLC and Innovative Display Technologies LLC v. Sony Corp. et al.*, Case No. 1:13-cv-02111-UNA DDEL, on behalf of Sony Corp.
- *Funai v. Gold Charm Limited*, Case No. IPR2015-01468, on behalf of Petitioner Funai
- *Phoenix, LLC v. Exar et al.*, Case No. 6:15-CV-00436-JRG-KNM., on behalf of Exar et al.
- *MiiC v. Funai*, Case No. 14-804-RGA, on behalf of Funai
- *Delaware Display Group LLC v. Vizio*, Case No. 13-cv-02112-RGA, on behalf of Vizio
- ARRIS v. Sony, U.S. ITC Investigation No. 337-TA-1060, on behalf of Sony
- *BlueHouse Global, LTD. v Semiconductor Energy Laboratory Co. LTD.*, IPRs on behalf of BlueHouse Global, LTD
- *Phoenix, LLC v. Wistron Corp.*, Case No. 2:17-cv-00711-RWS, on behalf of Wistron Corp.
- *Ultravision v Absen et al.*, ITC Investigation No. 337-TA-1114, on behalf of Absen et al.
- *Viavi Solutions Inc. v Materion Corp.*, PGR2019-00017, on behalf of Viavi Solutions, Inc.
- *NEC v Ultravision*, IPR2019-01123 and IPR2019-01117, on behalf of NEC
- *Solas OLED Ltd., v. Samsung Display Co., Ltd., et al.*, Case No. 2:19-cv-00152-JRG, on behalf of Solas

- *Solas OLED Ltd. v. LG Display Co., Ltd. et al*., 6:19-CV-00236-ADA, on behalf of Solas
- *Neodron Ltd., v. Dell Technologies Inc. et al.,* Case No. 1:19-cv-00819-ADA (Lead Case), on behalf of Neodron

III. TECHNOLOGY BACKGROUND

15. Semiconductor devices are electronic components that exploit the electronic properties of semiconductor materials, such as silicon. Semiconductor materials are useful because their behavior can be easily manipulated by the addition of impurities, known as doping. Current conduction in a semiconductor occurs via mobile or "free" electrons and holes, collectively known as charge carriers. Doping a semiconductor such as silicon with a small proportion of an atomic impurity, such as phosphorus, greatly increases the number of free electrons or holes within the semiconductor (a doped semiconductor containing excess holes is called "p-type"; one containing excess free electrons is known as "n-type").

16. Electricity flows like water. For a linear element in the circuit, the quantities of Voltage (V), Current (I) and Resistance (R) are related. Ohm's law is I=V/R. The action is not unlike water flowing from your home through a garden hose when you are watering your garden.

17. The current (I) is the amount of flow per unit time. For water we use gallons per minute. For electricity we use Amperes or "Amps" which is coulombs per second. A coulomb signifies a certain quantity of charge, similar to a "dozen." A dozen, however, is only 12 of something. A coulomb is about 6,000,000,000,000,000,000 electrons. So the current (I) in amps is the number of coulombs of electrons (or holes) flowing through an element each second.

18. The voltage (V) is like the water pressure coming from your house. For water we use the pressure unit pounds per square inch. For electricity we use Volts; it is the potential energy per

unit charge (measured in Joules per coulomb). The harder we push (V), generally the more flow (I) we get.

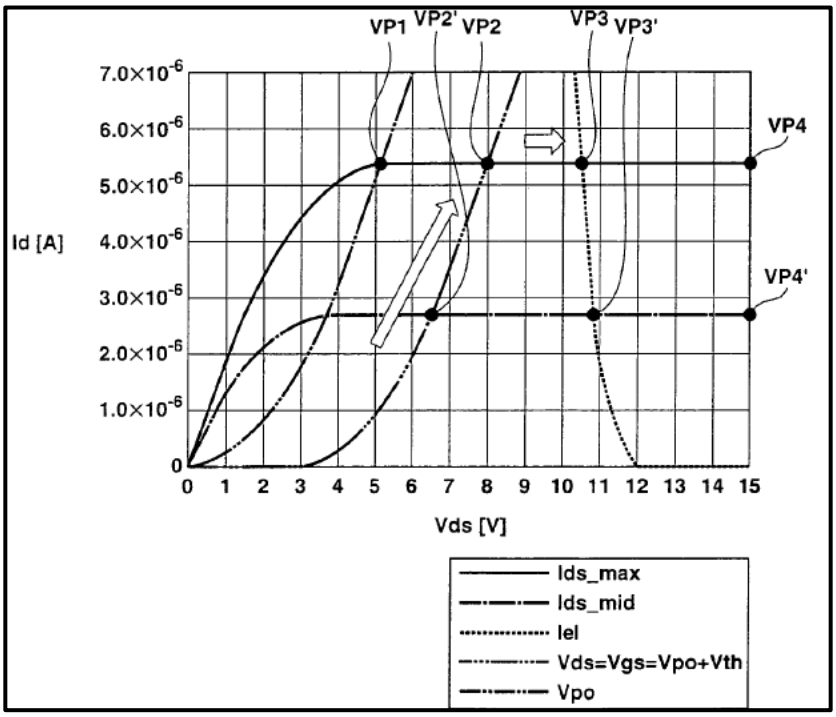
19. Resistance (R) is the resistance to flow. With water, the resistance comes from turbulent flow, viscosity, and friction between the water molecules and the pipe walls. With electricity, it comes from the material properties of the element in question and its dimensions. Electrical resistance is measured in ohms. I=V/R. A larger voltage (pressure) V creates a larger flow (current I). A larger R (resistance) lowers the flow (I) for any given applied voltage. In ordinary electronic devices, e.g. not using superconducting devices, no current will flow without a voltage being applied, just as no water will flow from a hose without pressure. Similarly, some movement of charges, i.e. a current, is necessary in order to apply a voltage in an electronic circuit.

20. For our garden hose, the water pressure from the house is a given. When we turn on the spigot, we get a certain flow. If the hose is kinked, additional resistance is introduced and the flow is reduced. On the other hand, with an unkinked hose, if the water company increases the water pressure, the flow increases.

21. Voltages and currents interact with each other in complex, but deterministic ways. Voltage and current are different entities, but are intrinsically inter-related. Ohm's law can be applied to linear electric elements, like resistors. Non-linear elements, like diodes and transistors, add additional aspects that must be considered.

22. A transistor (e.g. a thin film field effect transistor) is like a water spigot or gate valve. It can be turned fully off, partially on or fully on. The gate of a field effect transistor is like the handle on a water spigot. The level of voltage applied to the transistor gate regulates the current flow through the source/channel/drain of the transistor. There are threshold effects and saturation effects in transistors that produce their nonlinearity.

23. For example, below is the performance of a TFT shows the threshold voltage and nonlinear I-V characteristics, as described and taught in the ’068 patent:



24. An electric circuit, like the pixel circuit of an OLED display is a combination of nonlinear and linear devices, which electronically interact with each other. OLED display panels are currently used in high-end mobile phones, watches, televisions, and other products from a number of manufacturers.

25. Displays used in phones, watches, televisions, etc. contain a two-dimensional array of picture elements, commonly called pixels, that can each be controlled to produce a desired color and brightness of light. Together, these pixels form the desired image on the display. Each pixel is typically made up of a number of sub-pixels, commonly in colors red, green, and blue, corresponding to the three primary colors visible to most human eyes. By controlling the brightness of each sub-pixel, the brightness and color of an overall pixel can be controlled.

26. Unlike liquid crystal display technology, which uses a backlight, in OLED or other electroluminescent displays, each individual sub-pixel of the display directly emits light. OLEDs are current-controlled, meaning that the light emitted from each sub-pixel depends on the current that flows through the electroluminescent element in that sub-pixel. This means that each sub-pixel in the display has a circuit associated with it, commonly containing electronic components such as transistors and capacitors, which is responsible for sending the correct amount of current through the electroluminescent element and thus controlling the brightness of the sub-pixel.

III. BACKGROUND OF ASSERTED PATENTS

A. '450 Patent

27. The '450 patent teaches innovative designs for "active matrix" OLED displays with a high ratio of the area of the light emitting elements to the overall display area. The invention allowed the development of displays with high brightness, long life, and without various forms of performance degradation that plagued prior art designs. '450 patent at 2:66–3:7, 4:19–25, 9:9–19.

28. The '450 patent explains that prior art displays were either "passive matrix" OLEDs (i.e. no active elements at each pixel) or were "active matrix" OLEDs (i.e. with active elements such as transistors at each pixel). Active matrix OLED often used a bottom emission design (see Section V.D.) deposited directly on the glass substrate. Because the TFTs, capacitors and driving electrodes occupy an area of the pixel and because it is necessary to keep light away from the TFTs, the usable area is low. This reduces the brightness and/or reduces the lifetime of the OLED layer. *See id.* at 1:58-2:32 and Fig. 22, 23.

29. The '450 patent discloses a new architecture to address these deficiencies comprising a top emission OLED design with an insulating layer and contact hole ("via") to connect to the array

substrate. Through this design (see *id.* at 5:23-6:44, Fig. 1 and 2, reproduced below), the useful area for OLED material is improved and the TFTs are shielded from any harmful light from the OLED layer.

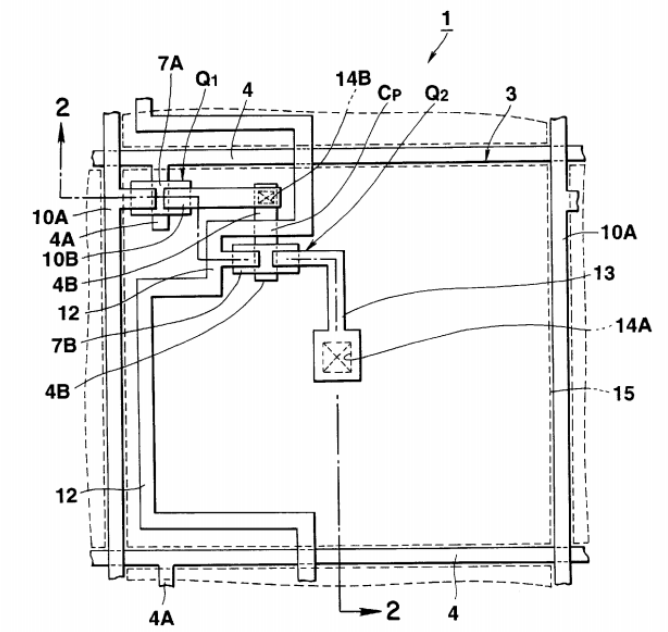


FIG.1

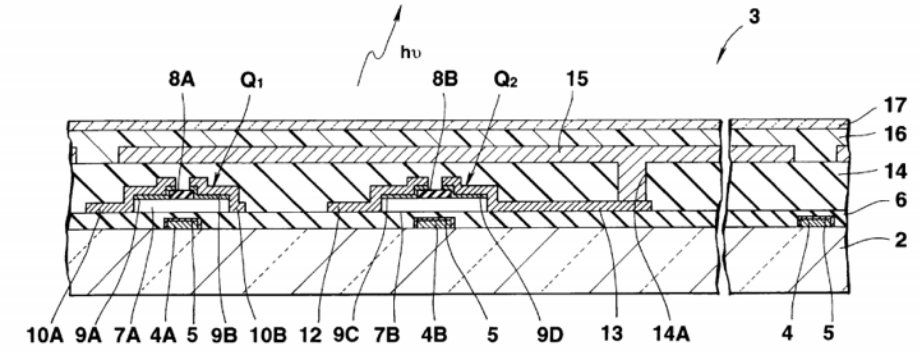


FIG.2

30. The active elements in the TFT array (Q1 and Q2) are a selection TFT and a drive TFT, respectively. A contact hole 14A is used to connect the cathode to the TFT array. The '450 patent describes the layers required to achieve the structure, as well as the interconnections of the layers

to achieve a working driving circuit. In addition, the '450 patent describes several embodiments for transistor architectures that use two TFTs and one capacitor, scan and data lines, and power supply line.

B. '338 Patent

31. The '338 patent concerns display panels with light-emitting elements, such as organic electroluminescent display panels. '338 patent at 1:14–21. A commonly used organic electroluminescent display technology is the organic light emitting diode, or OLED. OLED display panels are currently used in high-end mobile phones, watches, televisions, and other products from a number of manufacturers.

32. Displays used in phones, watches, televisions, etc. contain a two-dimensional array of picture elements, commonly called pixels, that can each be controlled to produce a desired color and brightness of light. Together, these pixels form the desired image on the display. Each pixel is typically made up of a number of sub-pixels, commonly in colors red, green, and blue, corresponding to the three primary colors visible to most human eyes. By controlling the brightness of each sub-pixel, the brightness and color of an overall pixel can be controlled. An example of this layout of sub-pixels is shown in Figure 1 of the patent:

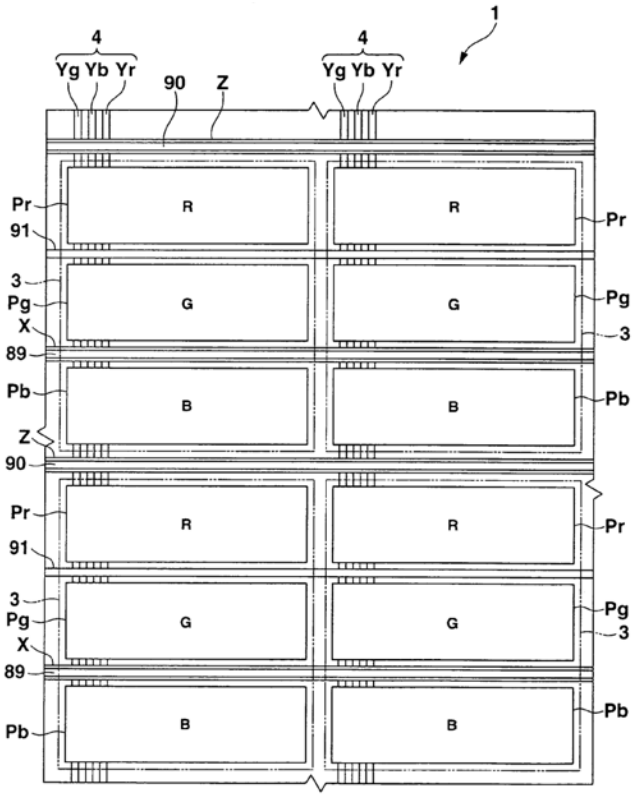


FIG.1

33. Unlike liquid crystal display technology, which uses a backlight, in OLED or other electroluminescent displays, each individual sub-pixel of the display directly emits light. OLEDs are current-controlled, meaning that the light emitted from each sub-pixel depends on the current that flows through the electroluminescent element in that sub-pixel. As the ’338 patent explains, the highest quality OLED displays are “active matrix.” ’338 patent at 1:19–21. This means that each sub-pixel in the display has a circuit associated with it, commonly containing electronic components such as transistors and capacitors, which is responsible for sending the correct amount of current through the electroluminescent element and thus controlling the brightness of the sub-pixel.

34. The ’338 patent shows an example sub-pixel circuit in Figure 2:

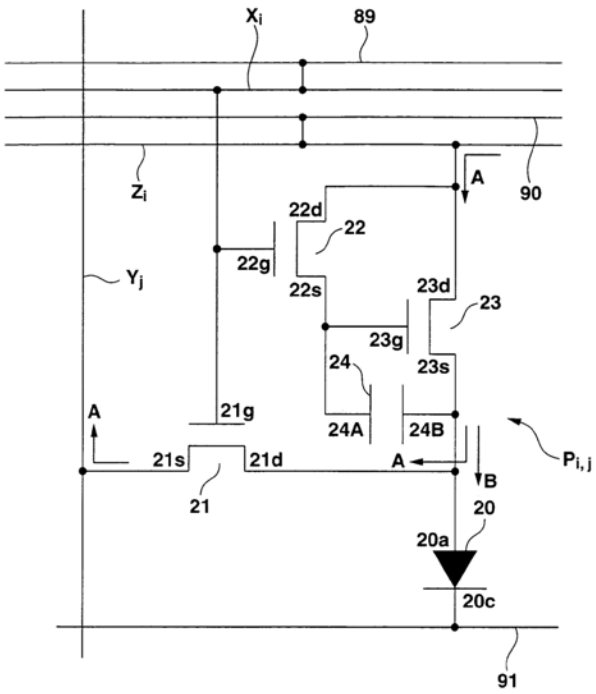


FIG.2

35. In this example circuit, the light-emitting element shown as the diode 20. The transistor 23 in this example is called the "driving transistor." During the time that the sub-pixel is emitting light, a "driving current" passes through the driving transistor and is supplied to the diode. '338 patent at 14:51–53. Periodically, the sub-pixel is selected to be written to by setting a voltage on the corresponding "scan line" X_i. '338 patent at 14:42–46. This voltage on the scan line turns the "switch transistor" 21 on. '338 patent at 16:30–32. Turning the switch transistor on permits a "write current" supplied by the "signal line" Y_i to pass through the circuit, particularly through the driving transistor. '338 patent at 14:59–63.

36. This flow of current causes a corresponding charge to form between the electrodes of the capacitor 24, and when the switch transistor is turned off, a current then flows through diode that depends on the charge on the capacitor, and in this example equals the write current. '338 patent at 15:54–16:13.

37. The patent specification describes a structure that implements a circuit of this type as a series of thin-film layers in the display panel, and the patent claims aspects of this structure.

C. '068 Patent

38. The '068 patent concerns improved designs for transistor array substrates, containing an array of "driving transistors" and associated lines and interconnections necessary to their operation. Such arrays of driving transistors are needed, for example, to drive active matrix displays utilizing organic electroluminescent elements. '068 patent at 1:24–36.

39. In prior art arrays, the materials, dimension, and arrangement of the transistor components and the lines and interconnections meant that the arrays suffered from undesirably large resistances and voltage drops, impairing the operation of driving transistors and the quality of the displayed image. The '068 patent teaches and claims improved designs for transistor arrays, with different arrangements of transistors, lines, interconnections, and electrodes, as well as with different dimensions or materials for such structures than those used in the prior art. E.g., '068 patent, Fig. 5.

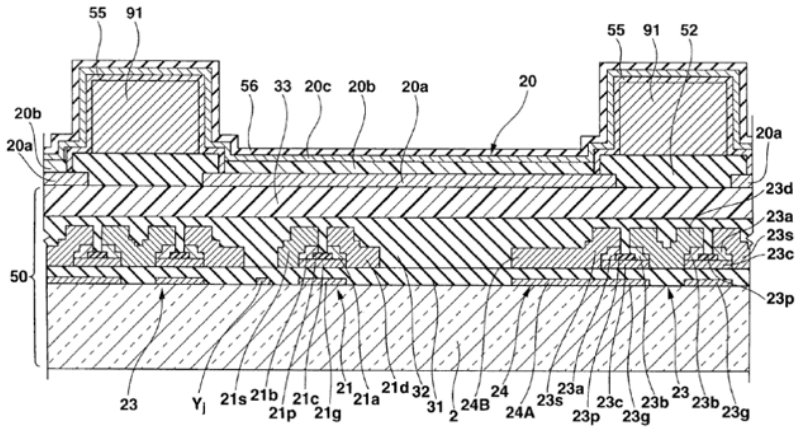


FIG.5

D. '042 Patent

40. The '042 patent addresses problems with active matrix OLED displays. *See* '042 patent at Background of the Invention. Specifically, the '042 patent recognizes that the transistors of such can vary or degrade over time, leading to inconsistent pixel brightness (*id.* at 2:7–28):

> Generally, the channel resistance of a transistor changes in accordance with a change in ambient temperature, or changes when the transistor is used for a long time. As a consequence, the gate threshold voltage changes with time, or differs from one transistor to another. Therefore, in the conventional voltage-controlled, active matrix driving type organic EL display in which the luminance and tone are controlled by the signal voltage, it is difficult to uniquely designate the current value of an electric current which flows through the organic EL element by the level of the gate voltage of the driving TFT, even if the current value of the electric current which flows through the organic EL element is changed by changing the level of the gate voltage of the driving TFT by using the signal voltage from the current line. That is, even when the gate voltage having the same level is applied to the driving TFTs of a plurality of pixels, the luminance of the organic EL element changes from one pixel to another. This produces variations in luminance on the display screen. Also, since the driving TFT deteriorates with time, the same gate voltage as the initial gate voltage cannot generate a driving current having the same current value as the initial current value. This also varies the luminance of the organic EL elements.

41. The ’042 patent addresses this problem by describing a display device with a plurality of selection scan lines, a plurality of current lines, and a data driving circuit. The driving circuit applies a reset voltage to the plurality of current lines and then supplies a designating current having a current value corresponding to an image signal. The pixel circuits then supply a driving current with a current value corresponding to the designating current which flows through the current lines. Importantly, the pixel circuits loads the designating current which flows through the current lines and stores a level of voltage converted in accordance with the current value of the designating current. After the selection period is over, the pixel circuits shut off the designating current and supplies a driving current corresponding to the level of the voltage converted in accordance with the designating current.

42. An exemplary embodiment of the ’042 patent invention is shown in Figure 1:

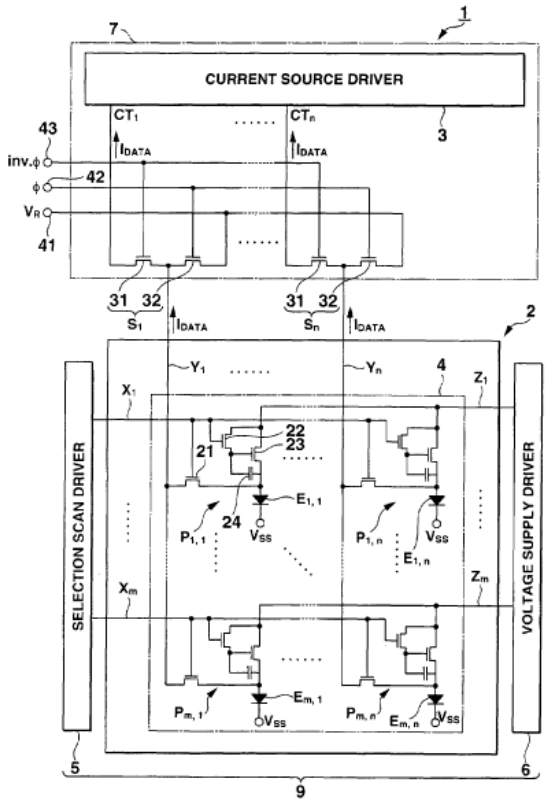


FIG.1

E. '615 Patent

43. The '615 patent concerns driving circuitry for self-luminous displays that emit light due to the current flowing through pixel elements, such as displays utilizing organic electroluminescent or LED elements. '615 Background of the Invention. The current flowing through such devices is commonly controlled by a gate voltage on a drive transistor. *Id.* However, the relationship between the gate voltage and the current may change "depending on the usage time, the drive history and the like," and in particular the minimum "threshold voltage" on the gate necessary to permit current flow may shift. *Id.* "For this reason," as the patent recognizes, "it becomes difficult to stably realize the light emission operation at the appropriate luminance gradation sequence in accordance with the display data for a long time." *Id.*

44. The '615 patent provides structures and methods for driving the pixel circuits that solve problems in the prior art, including through a light emission drive circuit that can apply a current control type (or a current drive type) of light emission element emitting light at a predetermined luminance gradation sequence by supplying a current in accordance with the display data to plural display panels (pixel arrays). Abstract. An exemplary embodiment is shown in Figure 15:

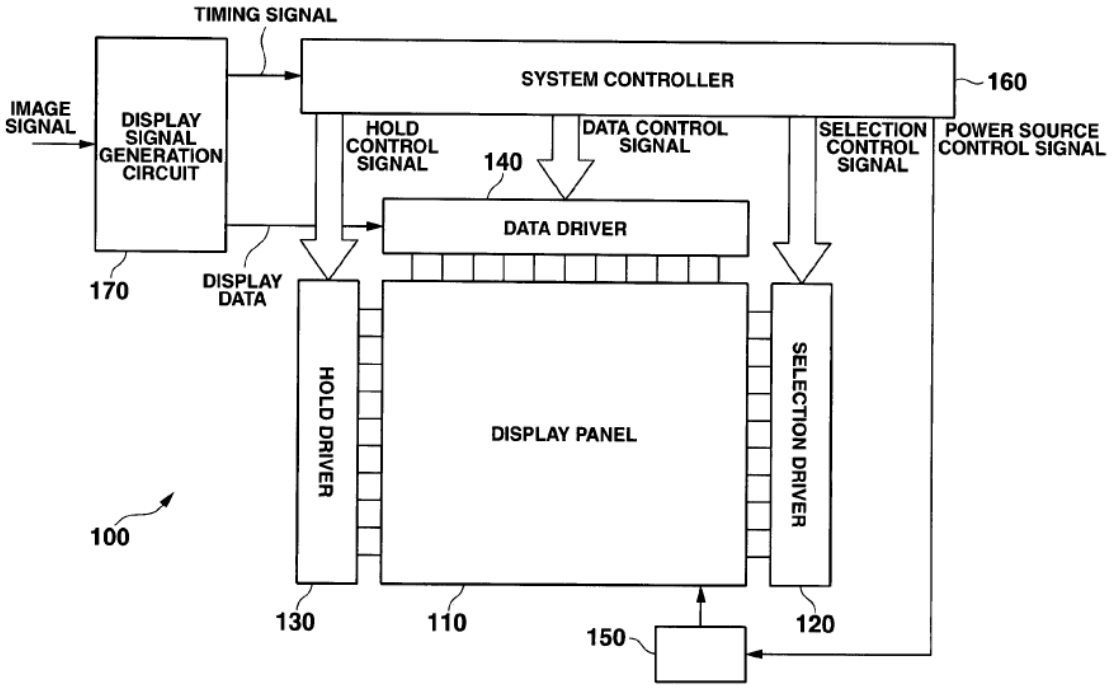


FIG.15

IV. LEVEL OF ORDINARY SKILL IN THE ART

45. In my opinion, a person of ordinary skill in the relevant art ("POSITA") for the Asserted Patents would be a person with a bachelor's degree in physics, electrical engineering, or a related field with approximately 3–5 years of experience in active-matrix and/or LED displays and systems, or a postgraduate degree such as a master's degree in physics, electrical engineering, or a related field with approximately 1–2 years of experience in active-matrix and/or LED displays

and systems. A person with less education but more relevant practical experience, or vice versa, may also meet this standard.

46. I further note that I am at least a POSITA and that for 50 years I have worked with colleagues who are POSITAs. Thus, I am well qualified to give technical opinions from the perspective of a POSITA.

V. CLAIM CONSTRUCTION PRINCIPLES

47. I understand that a claim construction inquiry begins and ends in all cases with the actual words of the claim. Thus, quite apart from the written description and the prosecution history, the claims themselves provide substantial guidance as to the meaning of particular terms. I further understand that to begin with, the context in which a term is used in the asserted claim can be highly instructive. The patent specification can also shed light on the meaning of claim terms.

48. I understand that when conducting a claim construction inquiry, district courts are not (and should not be) required to construe every limitation present in a patent's asserted claims. Simply put, claim construction is not an obligatory exercise in redundancy. I further understand that where a term is used in accordance with its plain meaning, the court should not re-characterize it using different language.

49. I understand that there is a "heavy presumption" that claim terms carry their full ordinary and customary meaning, unless the accused infringer can show the patentee expressly relinquished claim scope. The ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention. Thus, the task of comprehending the claims often involves little more than the application of the widely accepted meaning of commonly understood words.

50. I understand that without clear and unambiguous disclaimer, courts do not import limitations into claims from examples or embodiments appearing only in a patent's written description, even when a specification describes very specific embodiments of the invention or even only a single embodiment. Similarly, statements during patent prosecution do not limit the claims unless the statement is a clear and unambiguous disavowal of claim scope.

51. I understand that Defendant bears the burden of proving that a claim is indefinite by clear and convincing evidence. I understand that a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.

VI. AGREED TERMS

52. I understand that Solas and Defendants Dell Inc., Google LLC, Apple Inc., and HP Inc., (collectively "Defendants") have agreed to the constructions below.

A. '450 Patent

53. The following are the agreed terms for the '450 patent:

Claim Term / Asserted Claim(s)	Agreed Construction
"active elements" (claims 1, 4)	circuit elements that have gain or that direct current flow, e.g., transistors
"light lays [sic] in a first wavelength range pass through said at least one filter selectively when incident light rays in a second wavelength range including said first wave length range enter said at least one filter"	Plain and ordinary meaning. "lays [sic]" means and should be replaced with "rays"

Claim Term / Asserted Claim(s)	Agreed Construction
(claim 12)	

B. ’338 Patent

54. The following are the agreed terms for the ’338 patent:

Claim Term / Asserted Claim(s)	Agreed Construction
“the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate” (claim 1)	the pixel electrodes are arrayed along the interconnections and located between the interconnections, and the pixel electrodes are on the surface of the transistor array substrate
“write current” (claim 1)	pull-out current

C. ’068 Patent

55. The following are the agreed terms for the ’068 patent:

Claim Term / Asserted Claim(s)	Agreed Construction
“feed interconnections” (claims 1, 13)	conductive structures in a different layer or layers than the supply line that also provide connections to a source that supplies voltage and/or current
“patterned together [with]” (claims 1, 13)	“patterned to fit together [with]” wherein “patterning” may consist of one of more fabrication steps

D. '615 Patent

56. The following are the agreed terms for the '615 patent:

Claim Term / Asserted Claim(s)	Agreed Construction
"gradation" (claims 11, 13)	level
"light emission control section" (claim 11)	drive transistor

VII. DISPUTED TERMS FOR '338 PATENT

A. "transistor array substrate" ('338 patent claims 1, 4)

Solas's Proposed Construction	Defendants' Proposed Construction
layered structure upon which or within which a transistor array is fabricated	a layered structure composed of a bottom insulating layer through a topmost layer on whose upper surface pixel electrodes are formed, which contains an array of transistors

57. Defendants' proposed construction of "transistor array substrate" includes the terms "array of transistors." Likewise, Solas's proposal includes the phrase "transistor array." Thus, it appears that the parties do not believe that this part of the disputed phrase requires any construction. I agree—as it is a term of art with a clear plain and ordinary meaning to a POSITA.

58. Moreover, with respect to the term "substrate," it appears both sides agree it is a "layered structure." I agree with this as well. To a POSITA, every relevant substrate will be a layered structure. But beyond these points of agreement, Defendants' construction includes seventeen

more words—**"composed of a bottom insulating layer through a topmost layer on whose upper surface electrodes are formed"**—about what that layered structure requires. In doing so, the construction significantly departs from the plain meaning of the disputed term.

59. It is my opinion that Solas's construction is the only one to accurately capture the plain meaning of "transistor array substrate" as understood by a POSITA, in the context of the '338 patent. The transistor array substrate is a structure containing a transistor array. The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition (2000) is published by the Institute of Electrical and Electronics Engineers, a premier professional association for electronic and electrical engineering and associated disciplines and a publisher of technical standards. In the context of transistors and integrated circuits, this dictionary provides the relevant definition of substrate: "(1) (integrated circuit) The supporting material upon or within which an integrated circuit is fabricated or to which an integrated circuit is attached." Solas's proposed construction of "layered structure upon which or within which a transistor array is fabricated" is consistent with this definition.

60. Defendants' proposed construction, on the other hand, redefines "transistor array substrate" –and, in particular, the term "substrate"—to require a particular formation of electrodes and to require that formation occur on an "upper surface." Essentially, Defendants rewrite "transistor array substrate" as "electrode substrate." This is not how a POSITA would understand the term. A POSITA would understand that a "transistor array substrate" does not necessarily, by definition, have electrodes formed on it, let alone that the electrodes are necessarily formed on the "upper surface."

61. Nothing in the specification or the prosecution history defines "transistor array substrate" in a way different from its ordinary meaning or disclaims any form of transistor array substrate.

62. Defendants may argue that "transistor array substrate" is defined by the sentence from the specification: "The layered structure from the insulating substrate **2** to the planarization film **33** is called a transistor array substrate **50**." '338 patent at 10:45–47. Defendants may also point to the sentence: "The plurality of sub-pixel electrodes **20**a are arrayed in a matrix on the upper surface of the planarization film **33**, i.e., the upper surface of the transistor array substrate **50**." '338 patent at 11:50–52. As understood by a POSITA, neither of these sentences defines the term "transistor array substrate."

63. Both of these sentences are in the "Detailed Description of the Invention" section which describes a "best mode for carrying out the present invention," but also says the invention is "not limited" to the embodiment described in the section. '338 patent at 4:42–50. The quote from lines 10:45–47 of the specification simply says that in the specific example of Figure 6 (see '338 patent at 8:18–20), the layers from **2** through **33** are called the transistor array substrate. It does not define a transistor array substrate or say that a transistor array substrate necessarily contains specific layers from Figure 6.

64. Even if lines 10:45–47 could be interpreted as defining "transistor array substrate," they do not define it the way that Defendants propose. Lines 10:45–47 talk about layer 2, layer 33, and the layers in between. Defendants propose defining "transistor array substrate" based on where a different layer, the electrodes (e.g., sub-pixel electrodes **20**a in Figure 6), is located. Nowhere does the '338 patent define "transistor array substrate" that way.

65. The sentence from lines 11:50–52 simply points out that in the example of Figure 6, the upper surface of the planarization film happens to also be the upper surface of the transistor array substrate. It does not define the phrase "planarization film" in terms of the phrase "transistor array

substrate," or vice versa. It also does not define either of them in terms of where the "sub-pixel electrodes" are located.

66. This is further demonstrated by another similar sentence in the specification: "An insulating line **61** parallel to the scan line X is formed on the surface of the planarization film **33**, i.e., on the surface of the transistor array substrate **50**." '338 patent at 10:48–50. If lines 11:50–52 defined "transistor array substrate" in terms of the sub-pixel electrodes, then lines 10:48–50 would define "transistor array substrate" in a different way, in terms of the insulating line. A POSITA would not understand the patent to be providing two different definitions for "transistor array substrate" in lines 10:48–50 and lines 11:50–52. Instead, a POSITA would understand that these sentences are doing nothing more than describing the relationships between certain layers in an example embodiment of the invention. Each of the sentences at lines 10:45–47, lines 10:48–50 and lines 11:50–52 of the specification is consistent with the plain and ordinary meaning of "transistor array substrate," which is the construction that Solas has proposed.

67. Further evidence that the specification does not define "transistor array substrate" in the way suggested by the Defendants is found in an alternative "top emission" embodiment discussed in the '338 patent specification at 11:66–12:5. The embodiment in Figure 6 is a "bottom emission" device, and the language in lines 10:45–47 of the specification are in the context of a describing that bottom emission structure. '338 patent at 10:42–47.

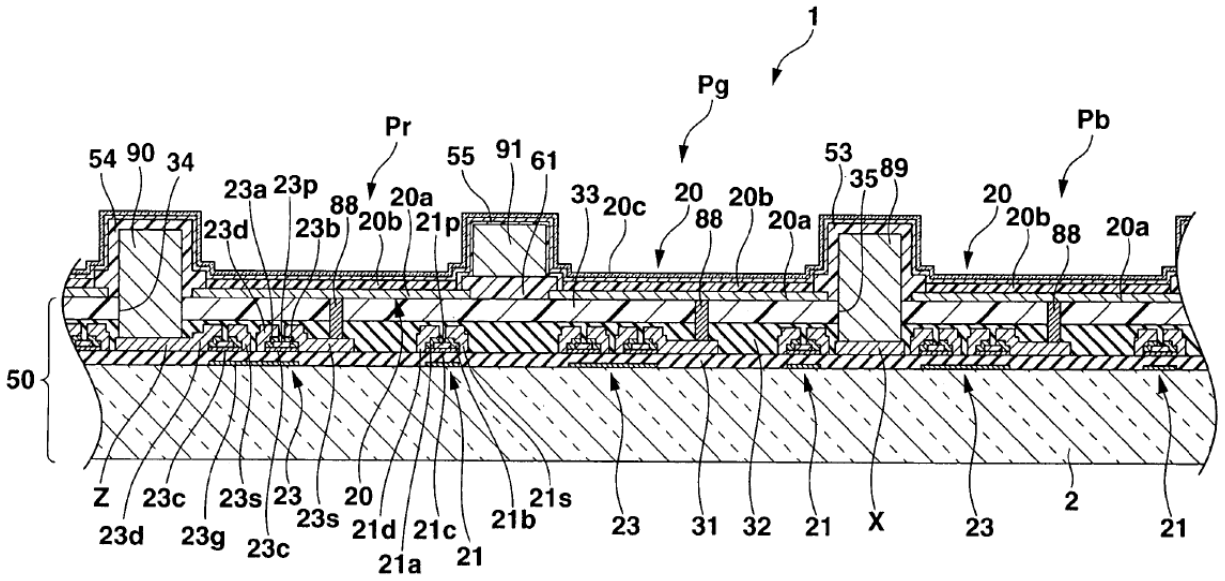


FIG.6

68. As the name suggests, in this "bottom emission" device the light emitted from the light-emitting layers leaves the device traveling downward (toward the bottom of the page in Figure 6). The counter electrode 20c above the light-emitting layers is described in the specification as being made from a metal that reflects light from the light-emitting layers downward. '338 patent at 13:42–46. The patent also describes a "top emission type" device. '338 patent at 11:66–12:5. In that device, the counter electrode 20c is made of a transparent material such as indium tin oxide (ITO), and "a reflecting film having high conductivity and high visible light reflectance is preferably formed between the sub-pixel electrode 20a and the planarization film 33." '338 patent at 12:1–3, 13:57–61.

69. If we treat the sentence as lines 10:45–47 as a definition of "transistor array substrate," then the transistor array substrate still ends at the planarization film 33 and does not include this added reflecting film in the top emission alternative. To the extent that Defendants intend their proposed construction to require that the pixel electrodes are formed directly on the transistor array

substrate surface, without any layers in between, the transistor array substrate would have to include the reflecting film. In that case, Defendants' proposed construction does not match the statement at lines 10:45–47 or any statement in the patent defining "transistor array substrate."

70. A POSITA would understand that in some contexts a reflecting film may be considered part of the transistor array substrate, and in other contexts it may not. A POSITA would recognize that any layered structure upon which or within which a transistor array is fabricated could be considered a transistor array substrate. A POSITA would also understand that within a given structure, there may be more than one set of layers that could be identified as constituting the "transistor array substrate."

71. I have reviewed the extrinsic evidence cited by Defendants, and it is consistent with my opinions. The patents 7,573,068 and 7,498,733 are other patents that share inventors with the '338 patent and describe inventions with preferred embodiments that are similar to the preferred embodiment of the '338 patent. In describing these embodiments, they contain similar statements, such as "The layered structure from the insulating substrate **2** to the planarization film **33** is called a transistor array substrate **50**." 7,573,068 patent at 10:34–35; 7,498,733 patent at 8:47–49. For the same reasons this sentence is not a definition of "transistor array substrate" in the '338 patent, it is also not a definition in these other two patents. A sentence describing features of preferred embodiments does not become a definition simply because it appears in more than one patent.

72. Defendants also cite a definition for "substrate" from The New Oxford American Dictionary, Second Edition:

sub·strate /'səb,strāt/ ▶*n.* a substance or layer that underlies something, or on which some process occurs, in particular: ■ the surface or material on or from which an organism lives, grows, or obtains its nourishment. ■ the substance on which an enzyme acts. ■ a material that provides the surface on which something is deposited or inscribed, for example the silicon wafer used to manufacture integrated circuits. ▷early 19th cent.: anglicized form of SUBSTRATUM.

73. In my opinion, this dictionary definition does not reflect the relevant plain and ordinary meaning to a POSITA as accurately as the IEEE dictionary I discuss above. The dictionary is not a technical dictionary, and the definition gives examples from biology that are irrelevant to the technology of the '338 patent. But even this definition does not support Defendants' position: that a "transistor array substrate" is by definition a surface where "electrodes" are formed.

B. "project from a surface of the transistor array substrate" ('338 patent claim 1)

Solas's Proposed Construction	Defendants' Proposed Construction
extend beyond an outer surface of the transistor array substrate	extend **above the upper surface** of the transistor array substrate

74. Solas's proposal matches the construction adopted by Judge Gilstrap in the *Solas v. Samsung* case, Case No. 2:19-cv-00152. I have highlighted in bold the text that differs between the two proposed constructions. Defendants' proposed construction replaces the word "beyond" from Judge Gilstrap's construction with the word "above" and replaces the phrase "an outer surface" with "the upper surface."

75. In my opinion, a POSITA would understand the phrase to have the meaning Solas has proposed, in the context of the '338 patent. The phrase "extend beyond" has a clear meaning. "Extend above" does not in any way make the construction clearer. The specification never refers

to anything extending or projecting "above" something else. Defendants' proposal simply rewords the claim term, without any support for doing so in the '338 patent itself.

76. Defendants' proposal also replaces the phrase "an outer surface" with "the upper surface." While the claim allows the interconnections to project from any "surface" of the transistor array substrate, Defendants' proposal requires that they project specifically from a specific "upper surface." Defendants appear to be taking a description of one preferred embodiment from the specification and importing that as a requirement of the claims. Specifically, the specification states that "the select interconnection **89** and feed interconnection **90** project upward from the upper surface of the planarization film **33**." '338 patent at 11:39-41. But, other descriptions of interconnections leave out the word "upper," saying for example that "The common interconnection 91 . . . is therefore formed to . . . project upward from the surface of the planarization film 33." '338 patent at 10:54-58.

77. A POSITA reading the claims of the '338 patent in the context of the patent would understand that the claimed "a surface" of the transistor array substrate simply needs to be a surface of that substrate and that there is no need that it be a specific "upper surface," should the transistor array substrate have more than one surface. Nothing in the specification redefines "surface" to be "upper surface," and nothing in the specification or the file history that I have reviewed disclaims surfaces other than an "upper surface."

78. I have reviewed the extrinsic evidence cited by Defendants, and it is consistent with my opinions. Defendants cites a definition for "project" from The New Oxford American Dictionary, Second Edition:

▶*v.* /prə'jekt; prō'jekt/ [*trans.*] **1** (usu. **be projected**) estimate or forecast (something) on the basis of present trends: *spending was projected at $72 million.* ■ [often as *adj.*] (**projected**) plan (a scheme or undertaking): *a projected exhibition of contemporary art.* **2** [*intrans.*] extend outward beyond something else; protrude: *I noticed a slip of paper projecting from the book* | [as *adj.*] (**projecting**) *a projecting bay window.* See note at **BULGE**. **3** [*trans.*] throw or cause to move forward or outward: *seeds are projected from the tree.* ■ cause (light, shadow, or an image) to fall on a surface: *the one light projected shadows on the wall.* ■ cause (a sound, esp. the voice) to be heard at a distance: *being audible depends on your ability to project your voice.* ■ imagine (oneself, a situation, etc.) as having moved to a different place or time: *people may be*

79. The second verb definition in this dictionary uses the word "extend," which is a word that both Solas and Defendants use in their proposed constructions. But the definition does not say anything about extending "above" or about an "upper" surface, as Defendants' construction requires.

VIII. DISPUTED TERMS FOR '068 PATENT

A. "supply lines" ('068 patent claims 1, 13)

Solas's Proposed Construction	Defendants' Proposed Construction
conductive lines supplying current or voltage	conductive lines, each supplying a driving current or voltage to a plurality of pixel circuits

80. Solas's construction is correct and supported by the intrinsic evidence. I note it was the agreed construction in the Solas v. LG/Sony case. The '068 specification provides the following examples:

- During some period of time, the supply lines carry a voltage, VL. *See* '068 patent at 15:55 ("The feed driver sequentially outputs the write feed voltage VL of low level (lower than the voltage of the counter electrode of the organic EL elements 20) to the supply lines[.]").
- Sometimes the supply lines carry a higher voltage VH. *See id.* at 16:48–50 ("During the light emission period, the potential of the supply line Z, and the feed interconnection 90 connected to it equals the driving feed voltage VH.").
- Sometimes the supply lines carry a write current. *Id.* at 16:17 ("the write current (current signal) to the signal line Y, flows from the feed interconnection 90 and supply line Z, through the source to-drain path of the driving transistor 23").
- Sometimes the supply lines carry a driving current. *Id.* at 16:53 ("Hence, a driving current flows from the supply line Z, and the feed interconnection 90 connected to it to the organic EL element 20 in the direction of arrow B through the driving transistor 23.").

81. The '068 specification further makes clear that the "write current" and the "driving current" are not synonymous. *See id.* at 19:26–30 (referring to Fig. 15). Thus, at different times, the supply lines can carry various voltages and currents. This supports Solas's construction, which is the plain meaning of lines, i.e., "conductive lines supplying current or voltage."

82. Defendant's proposed construction "conductive lines, each supplying a driving current or voltage to a plurality of pixel circuits" is not the plain and ordinary meaning of "conductive lines." Further, it is unsupported and incorrect.

83. Defendants' construction is too limiting. It reads out portions of the preferred embodiment by ignoring the write current. Further, it imports limitations from portions of particular embodiments. That is, why must each supply line supply a plurality of pixel circuits? A POSITA would not understand this to be the case or always required. A POSITA would understand that the

term could include a single supply line connecting the feed interconnect and the drive transistor. I have reviewed the specification and prosecution history and do not find any lexicography or disclaimer that supports Defendants' construction.

B. "formed on said plurality of supply lines along said plurality of supply lines" ('068 patent claim 1) /

"connected to said plurality of supply lines along said plurality of supply lines" ('068 patent claim 13)

Term	Solas's Proposed Construction	Defendants' Proposed Construction
"formed on said plurality of supply lines along said plurality of supply lines"	formed on said plurality of supply lines over the length or direction of said plurality of supply lines	stacked on or making multiple contacts with said plurality of supply lines over the length of each supply line
"connected to said plurality of supply lines along said plurality of supply lines"	connected to said plurality of supply lines over the length or direction of said plurality of supply lines	stacked on or making multiple contacts with said plurality of supply lines over the length of each supply line

84. The '068 patent claims recite "a plurality of feed interconnections" which are "formed on" (claim 1) or "connected to" (claim 13) "said plurality of supply lines along said plurality of supply lines." Solas's construction is that along means "over the length *or direction* of." It is supported by the intrinsic evidence and was adopted by the Court in the Solas v. LG case. Defendants' construction changes the claim term in many unrecognizable and unsupported ways. Defendants' change "formed on" to "stacked on or making multiple contracts with" and change "along said plurality of supply lines" to "over the length of each supply line." Defendants incorporates LG's proposal from the LG case but adds other improper limitations.

85. The plain meaning of the claim language, as well as the intrinsic and extrinsic evidence, support Solas's proposed construction. The plain meaning of "along" is over the length or direction of. Dictionaries define along in precisely this way. *See* Ex. E (Merriam-Webster Dictionary)

("along: 1: in a line matching ***the length or direction of*** // walking *along* the river; *also*: at a point or points on // a house *along* the river"); Ex. F (Dictionary.com) ("along: 1 through, on, beside, over, ***or parallel to the length or direction of***; from one end to the other of: *to walk along a highway*."). To say that "I walked along the Mississippi River" does not mean that I walked over the length of the Mississippi River. Rather, it means that I walked in the direction of the Mississippi River over some portion of its length.

86. The claim language uses "along" consistent with this plain meaning. The claims recite a plurality of feed interconnections "formed on" or "connected to" a plurality of supply lines "along" the plurality of supply lines. A POSITA would understand that the feed interconnections are formed on or connected to the supply lines over the direction of the supply lines. The claims do not require the feed interconnections to be formed or connected over the length of the supply lines—nor require the feed interconnections and supply lines to be the same length. Indeed, based the parties' proposals, the parties agree that feed interconnections are "conductive structures in a layer or layers" and that supply lines are "conductive lines." A POSITA would not understand that conductive structures need to be formed on or connected to conductive lines over the length of those lines. There is no lexicography that compels such extreme narrowing from the plain meaning. And Defendants have not pointed to any clear disclaimer of its invention from the prior art to warrant the narrowing it seeks, either.

87. The specification also supports Solas's construction. In describing an example of the overall arrangement of the display panel, it states that the feed interconnections and its common connections are provided "***in parallel to***" the supply lines. *See* '068 patent at 6:26 ("The feed interconnections 90 *are provided in parallel to the supply lines* Z_1 to Z_m when viewed from the upper side. The common interconnections 91 *are provided in parallel to the signal* lines Y_1 to Y_n

when viewed from the upper side."); *see also id.* at 23:1–6. This shows that the feed interconnections are formed on or connected to the supply lines at particular locations and that those locations are "parallel to" (in the direction of) the supply lines.

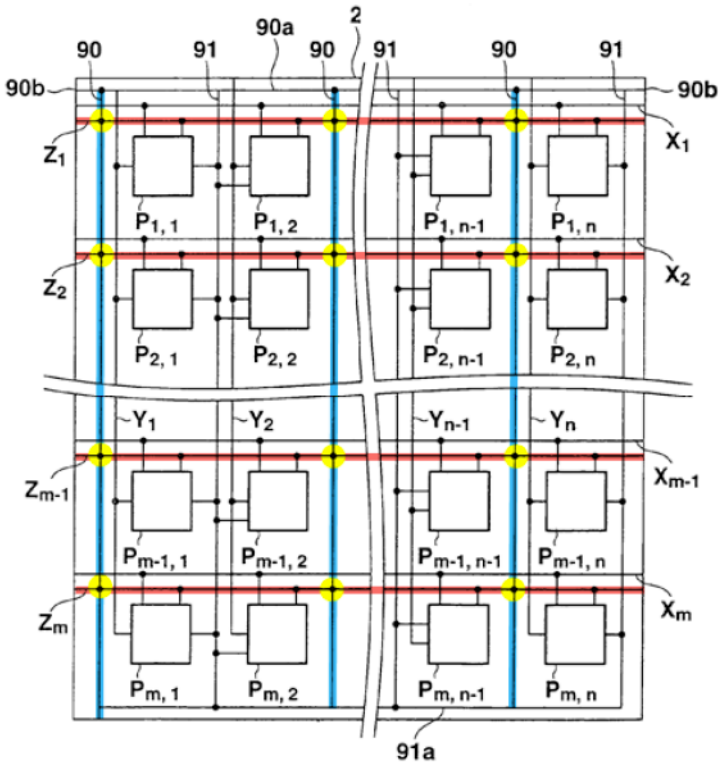
88. Further, the claim clearly refers to a plurality (a group of more than one) of feed interconnections and to a plurality (a group of more than one) of supply lines. The claim language does not place conditions, restrictions, or limitations on individual feed interconnects or individual supply lines. The patent discloses at least two relevant embodiments.

89. In this first embodiment (Figs. 1 and 2), each feed interconnections 90 runs parallel to and is connected to one of the supply lines (Zi). In fact, Fig 8 shows the feed interconnections formed directly on the top surface of the supply line Zi.

90. In the second embodiment (Figs. 20 and 21), each feed interconnection 90 crosses and connects to each supply line (Zi) at the crossovers C2. In this embodiment each feed interconnect runs along the plurality of supply lines at right angles. Therefore, the plurality of feed interconnects connects to and runs along the plurality of supply lines. The claim language is not referring to individual interconnections or lines. The claim language refers to pluralities.

91. Both embodiments comport with the claim language in both claim 1 and claim 13. A POSITA would understand this.

92. Defendants' proposed constructions require "stacked on or making multiple contacts with said plurality of supply lines over the length of each supply line" and are incorrect and too limiting. For example, as discussed, Fig 2 shows feed interconnects 90 and supply lines Z crossing at right angles. Therefore, there are embodiments where the feed interconnect is neither stacked on nor having multiple contacts . . . over the length of each supply line."



93. This embodiment is consistent only with Solas's construction because the interconnections run "over the length or direction of" the supply lines. They do not, as Defendants' *construction* might suggest, run just over the length of the supply lines. And they certainly do not, as Defendants' possible interpretation of their construction suggests, run "over and throughout the entire length of" or "for the length of." Nor do they require each interconnect to make "multiple contacts with" the supply lines "over the length of each supply line."

94. In sum, Defendants' constructions are incorrect because they are not the plain meaning and because there is no lexicography or disclaimer that requires them. For example, the specification and prosecution history do not redefine "along" to mean Defendants' constructions. Nor do they require the feed interconnections to be "stacked on or making multiple contacts with said plurality of supply lines over the length of each supply line" I have reviewed the intrinsic evidence and found no lexicography or disclaimer that supports Defendants' constructions.

C. "signal lines" ('068 patent claims 1, 13)

Solas's Proposed Construction	Defendants' Proposed Construction
conductive lines supplying signals	conductive lines carrying data

95. The parties agree that the "signal lines" are conductive lines . Solas's construction correctly follows the plain meaning of the term, by requiring that the signal lines supply "signals." This is how the term is used in the '068 patent. For example, specification describes at 1:38–45: "a voltage of level representing the luminance is applied to the gate of the driving transistor through a signal line." The specification also describes at 16:14–21: "As shown in FIG. 2, a write current (current signal) having a current value corresponding to the gray level is supplied from the data driver to the signal lines Y to Y, as indicated by an arrow A." Both examples are consistent with Solas's construction in that the signal lines supply signals where the signal can sometimes be a voltage and sometimes a current. The patent's usage is also consistent with dictionary definitions of "signal." MS Dict. at 435 ("signal *n.* 1. Any electrical quantity, such as voltage, current, or frequency, that can be used to transmit information")

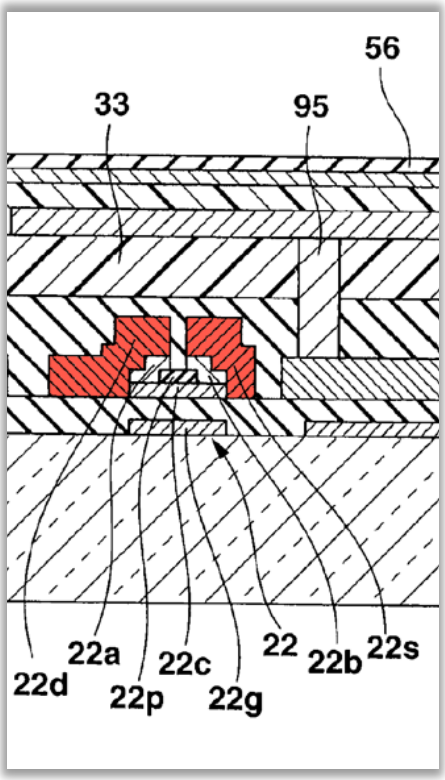
96. Defendants propose a different construction, requiring that signal lines "carry data." But nothing in the claims or specification require "carrying data" or suggests that the invention should be limited to "signal lines" carrying data. In my opinion, Defendants' construction is not equivalent or commensurate with the plain meaning of the term. Nothing in the specification or file history provides a special definition of "signal lines" or a disclaimer or lexicography that supports Defendants' construction. Defendants' proposal may also lead to confusion and ambiguity and disputes about the meaning of "data." Indeed, in another patent, the term "data lines" is a disputed term for construction.

D. "source" / "drain" ('068 patent claims 1, 5, 12, 13, 17)

Term	Solas's Proposed Construction	Defendants' Proposed Construction
"source"	Plain and ordinary meaning	source electrode
"drain"	Plain and ordinary meaning	drain electrode

97. The '068 patent states at 1:63: "More specifically, in manufacturing the display panel, a conductive thin film as a prospective electrode of a thin-film transistor is subjected to photolithography and etching to form the electrode of a thin-film transistor from the conductive thin film." In general, the '068 never uses the terminology "source electrode" or "drain electrode." The 068 in numerous places uses the term "gate electrode." This is easily understood because indeed the gate is a metal conductive film, so the use of "gate electrode" is routine.

98. The '068 is clear. In explaining Fig 8, at 8:47 it states: "The drain 22d is formed on one impurity-doped semiconductor film 22a. The source 22s is formed on the other impurity-doped semiconductor film 22b. The drain 22d and Source 22s can have either a single-layer structure or a layered structure including two or more layers."



99. And at 8:64 the specification states: " The drain 23d is formed on one impurity-doped semiconductor film 23a. The source 23s is formed on the other impurity-doped semiconductor film 23b. When viewed from the upper side, the source 23s of the driving transistor 23 has a U shape so that the channel width of the driving transistor 23 is large. The drains 21d to 23d and sources 21s to 23s of the transistors 21 or 23 are formed by patterning the same material layer."

100. So in the '068 patent, the source and drain comprise patterned conductive films that connect the TFT channel ends to other circuit elements (like the pixel electrode or data lines). Defendants' proposed insert of "electrode" is unsupported, ambiguous, and may itself require further construction. For example, the term "electrode" has different meanings in electrochemistry, batteries, and some circuits. It would be inappropriate to include another word, not supported by the intrinsic evidence, as part of construing "source" and "drain."

101. A POSITA would understand that the "source" and "drain" are common terms to persons of ordinary skill and does not require further construction. For example, a POSITA would know that in TFTs, the structure is symmetric with respect to source and drain. At one end of the channel region is the source and the other end is the drain. In other words, a POSITA would know that the source (or drain) is the patterned conductive film that is connected to one end of the TFT channel region through a doped semiconductor region. A POSITA would not require importing the word "electrode" as part of the meaning of source or drain.

102. I have also reviewed several dictionary definitions of "source" and "drain" that support my opinions above and confirm that the terms do not require further construction. These definitions also undercut Defendants' attempt to impose the additional word "electrode." These exemplary definitions are:

- IEEE at 337 (drain: "Region in the device structure of an insulated-gate field-effect transistor (IGFET) which contains the terminal into which charge carriers flow from the source through the channel. It has the potential which is more attractive than the source for the carriers in the channel."), 1074 (source: "Region in the device structure of an insulated-gate field-effect transistor (IGFET) which contains the terminal into which charge carriers flow into channel toward the drain. It has the potential which is less attractive than the source for the carriers in the channel.")
- McGraw-Hill at 577 ("The region into which majority carriers flow in a field-effect transistor; it is comparable to the collector of a bipolar transistor and the anode of an electron tube."), 1777 ("The terminal in a field-effect transistor from which majority carriers flow into the conducting channel in the semiconductor material.").

IX. DISPUTED TERMS FOR '042 PATENT

A. "selection period" ('042 patent claim 1)

Solas's Proposed Construction	HP's Proposed Construction
time period during which a plurality of pixel circuits is selected	time duration in which a selected selection scan line is kept active

103. Solas's proposed construction of "selection period" accords with the plain and ordinary meaning of the phrase as described in the intrinsic record. For example, the specification explains referring to Fig. 4 that: "A period in which the selection scan driver 5 . . . and selects the selection scan line Xi in the ith row ***is called a selection period*** T_{SE} of the ith row." '042 Patent at 9:22-27 (emphasis added). patent further teaches: the "selection scan line" comprises "a plurality of pixel circuits." *Id*. at 2:46-48 (Brief Summary of Invention: "a plurality of pixel circuits which are connected to the plurality of selection scan lines"); at 3:17-20 (Brief Summary of Invention: "A display panel driving method according to still another aspect of the present invention comprises, a selection step of sequentially selecting a plurality of selection scan lines of a display panel comprising a plurality of pixel circuits"); ("In the second transistor 22 of each of the pixel circuits Di,1 to Di,n in the ith row, a gate 22 g is connected to the selection scan line Xi in the ith row").

104. The intrinsic record, including Figure 4 and related description confirms that the "selection period" is a *period* (consistent with Solas's proposal) not a *duration* (under HP's proposal). The "selection period" refers to a particular block of time having a specific beginning (e.g., T1) and a specific end (e.g. T2). Defendant's proposed use of "duration" is inappropriate, since a duration simply specifies a difference between two times (e.g., T1-T2) without specifying the specific values of T1 and T2, or the relationship between T1 and T2 and the rest of the signal and voltage

timings. For example, the 19th century and the 20th century are different time periods, even though they have the same duration (100 years).

105. Further, HP's proposal is also flawed because the "kept active" language is also inconsistent with the plain and ordinary meaning of the term "selection period." There is no disclosure in the specification that "selecting" a scan line entails some sort of "activation" The phrase "kept active" is vague and meaningless in this context. It is unclear whether HP suggests "active" means not deactivated or not "passive," or both. In any event one of skill in the art would reject adding this confusing and imprecise limitation to the term "selection period." Further, I have reviewed the intrinsic evidence and do not see any lexicography or disclaimer that would support HP's proposal.

B. "sequentially selects said plurality of selection scan lines in each selection period" ('042 patent claim 1)

Solas's Proposed Construction	HP's Proposed Construction
Plain and ordinary meaning	selects said plurality of selection scan lines one per each of a plurality of non-overlapping selection periods

106. A POSITA would understand every word of this claim phrase and understand that no further construction is required. The phrase consists of words that have a clear meaning to a POSITA. I address "selection period" above. The remaining terms have a plain and ordinary meaning and the specification uses these terms in accordance with their plain and ordinary meaning. For example, Merriam Webster's defines "sequential" as "following in sequence." Ex. 9. Synonyms are "consecutive" and "succeeding." *Id*. Dictionary.com similarly defines "sequence" as "the following of one thing after another; sequential" and "sequential" as

"following; subsequent; consequent." Ex. 10. The term has a simple and consistent plain and ordinary meaning and the '042 patent does not restrict, limit or change these meanings.

107. HP's proposal removes the claim language "sequentially" and "in each selection period" and replaces the simple terms with limitations that go beyond the meaning of the language—"one per each of a plurality of non-overlapping selection periods." There is no disclosure in the intrinsic record limiting the selection of the "plurality of scan lines" to "one per each of a plurality of" selection periods. Moreover, while for one or more embodiment, the certain selection periods are not described to overlap, there is no limitation of the phrase "in each selection period" to mean that no selection period may overlap under any circumstance. HP's proposal is incorrect and unsupported. I have reviewed the intrinsic evidence and found no lexicography or disclaimer that supports HP's proposed construction.

C. "designating current" ('042 patent claim 1)

Solas's Proposed Construction	HP's Proposed Construction
Plain and ordinary meaning, i.e., current designating a value corresponding to an image signal	current having a specified current value that is held constant

108. The term "designating current" has a plain and ordinary meaning to a POSITA and the '042 patent uses the term consistent with this plain and ordinary meaning, i.e., current designating a value corresponding to an image signal. This is how the term is explained throughout the '042 patent and the specification. For example, it is supported by the Abstract and Summary of the Invention, which uses the same language.

109. HP's proposal imposes an additional requirement that the designating current have "a specified current value that is held constant." There is no disclosure in the specification defining the designating current in this way. To the contrary, the specification never describes the

designating current as held constant during the first reset portion. *See* '042 patent at 11:54–59, 2:40–45. Further, Claim 1 itself describes that the "designating current" changes and is a value corresponding to an image signal. *See, e.g.*, '042 Patent Claim 1 ("wherein in the selection period, each of said plurality of pixel circuits loads the designating current which flows through said plurality of current lines"). This does not declare that during the whole selection period the designating current is held constant. In fact, we know from the specification that the designating current in one embodiment is held constant only during the second portion of the selection period. This is consistent with the claim language, and completely inconsistent with the HP's requirement proposed construction. HP's proposal reads out a preferred embodiment. I understand that such construction are rarely, if ever, correct.

D. "current lines" ('042 patent claim 1)

Solas's Proposed Construction	HP's Proposed Construction
Plain and ordinary meaning, i.e., conductive lines for carrying current	conductive lines, each connected to a plurality of pixel circuits and carrying current

110. The term "current lines" has a plain and ordinary meaning in the art and the '042 patent uses the term "current lines" in accordance with its plain and ordinary meaning, i.e., conductive lines for carrying current. HP appears to agree this is the plain and ordinary meaning of "current lines" but adds limitations about pixel circuits.

111. It is unnecessary to include pixel circuits as part of the construction of "current lines." Claim 1 already specifies that the claimed configuration is limited to a device having current lines connected to pixel circuits (reciting "a plurality of pixel circuits which are connected to said plurality of selection scan lines and said plurality of current lines"). Thus, only devices having

pixel circuits and current lines are claimed. HP's proposed construction requiring the conductive lines to be connected to pixel circuits is at best superfluous and should be rejected on that basis.

112. But HP's proposal is even narrower and substantively wrong. HP's additional limitations of "each connected to a plurality of pixel circuits" are not supported by the specification, which for example, describes that "a plurality of pixel circuits [] are connected to . . . the plurality of current lines." '042 Patent, Abstract. The specification does not state that each ***individual*** conductive line must be connected to a plurality of pixel circuits. HP's construction is incorrect and unsupported. I received the specification and prosecution history and do not find any lexicography or disclaimer that supports HP's construction requiring "current lines" to have "each [line] connected to a plurality of pixel circuits and carrying current."

X. DISPUTED TERMS FOR '615 PATENT

A. "the operation" ('615 patent claim 11)

Solas's Proposed Construction	HP's Proposed Construction
Plain and ordinary meaning, not indefinite. Within the claim phrase "a drive voltage for making the light emission control section perform the operation," the term "the operation" refers to "generating a light emission drive current having a predetermined current value in accordance with the electric charges accumulated in the electric charge accumulating section and supplying the light emission drive current to the light emission element."	Indefinite

113. A POSITA would understand the meaning and scope of the term "the operation" within the claim phrase "a drive voltage for making the light emission control section perform **the**

operation," with reasonable certainty in view of the claims, specification, and prosecution history. Specifically, claim 11 recites, in context:

> **11**. A display unit comprising:
> a plurality of display pixels each of which includes a light emission element and a light emission drive circuit having an electric charge accumulating section for accumulating electric charges based on a gradation sequence signal to designate a luminance gradation sequence in accordance with display data, a light emission control section for generating a light emission drive current having a predetermined current value in accordance with the electric charges accumulated in the electric charge accumulating section and supplying the light emission drive current to the light emission element, a writing control section for controlling a supplying state of the electric charges based on the gradation sequence signal to the electric charge accumulating section, and a voltage control section for controlling a drive voltage for making the light emission control section perform the operation, respectively;

114. Claim 11 describes "a light emission control section" for the first time and then immediately states its performed function: "for generating a light emission drive current having a predetermined current value in accordance with the electric charges accumulated in the electric charge accumulating section and supplying the light emission drive current to the light emission element." Later on in the same clause, the claim recites "a drive voltage for making the light control section perform ***the operation***." A POSITA would readily understand that "the operation" is referring to the operation of the recited "light emission control section." And that operation is unambiguous and was mentioned earlier in the same paragraph: "generating a light emission drive current . . . and supplying the light emission drive current to the light emission element."

115. I do not understand that HP argues that the other occurrences of "the operation" in claim 11 are indefinite. Indeed, they are not. For example, the second occurrence of "the operation" is part of a longer phrase "*the operation* state of the writing control sections of the display pixels." And the third occurrence is part of a longer phrase "*the operation* state of the voltage control sections of the display pixels." A POSITA of understand that these longer phrases are not indefinite and inform with reasonable certainty the scope of the claim. Further, the use of "the operation" in the second and third occurrences are as a noun adjunct, rather than a noun. A POSITA would understand the intended meaning of these claim phrases in view of claim 11 itself. *See, e.g.,* '615 patent at 48:34–36 (". . . a writing control section for controlling a supplying state of the electric charges . . . to the electric charge accumulating section . . ."); 48:37–48 ("a voltage control section for controlling a drive voltage . . ."); *see also* columns 4 and 5.

116. In every occurrence of the "operation" in claim 11, a POSITA would easily understand the intended meaning in every case, given the context and surrounding claim language. This understanding is further supported by the specification and prosecution history. *See, e.g.,* '615 patent at Summary of the Invention; Figs. 2, 3A, 3B, 4A, 4B, 10, 11A, 11B, 12A, 12B, 13, 14A, 14B (and written description associated with those figures).

B. "precharge voltage" ('615 patent claim 11)

Solas's Proposed Construction	HP's Proposed Construction
Plain and ordinary meaning	Indefinite

117. A POSITA would understand the meaning of precharge voltage with reasonable certainty in view of the claims, specification, and prosecution history. Claim 11 itself explains what the "precharge voltage" is. It states that "with respect to each of the display pixels, the data driver applies a ***precharge voltage*** exceeding a threshold value of the drive transistor to the data line, and

the light emission drive circuit applies the ***precharge voltage*** applied to the data line to the electric charge accumulating section via the writing control section." Therefore, the claim explains that the precharge voltage exceeds a threshold value of the drive transistor and is applied by the data driver to the data line. Further the specification gives detailed explanations about the function, magnitude, and timing of the precharge voltage. *See, e.g.,* '615 patent at 7:28–38 ("a first potential difference step of setting a first potential difference on the basis of a precharge voltage that is larger than the minimum luminance gradation sequence necessary for generating the light emission drive current required for making the light emission element to perform the light emission operation at the minimum luminance gradation sequence or a threshold potential difference between the control terminal and one end of a current path of the drive transistor in which a current value of the light emission drive current is set by a potential difference between a control terminal and one end of the current path"); *see also id.* at 7:58–61, 8:30–32 Fig. 2 ("a timing chart showing a first example of the drive control operation of the light emission drive circuit according to the embodiment"); Fig. 13 ("a timing chart showing a third example of the drive control operation of the light emission drive circuit according to the embodiment").

118. Based on these teachings, a POSITA would readily understand that the precharge voltage, as taught in the specification is the voltage applied to the data line to compensate for the drive transistor Tr13 transistor threshold voltage and to avoid the "dead spot" as the bottom of the grayscale curve as shown in fig 8. In other words, a POSITA would understand that the precharge voltage is a component of the Gradation Sequence Signal to enhance pixel brightness accuracy.

119. HP's indefiniteness argument is unsupported and inadequately explained. To the extent HP or its expert provide additional argument, I reserve the right to respond. For example, HP appears to complain that the patent provides additional details or examples about the precharge voltage

and contends they are "mutually exclusive." But the existence of multiple examples, even if allegedly mutually exclusive, does not show a claim term is indefinite. Further, it is not clear what HP contends are examples of the precharge voltage. To the extent HP articulates or identifies its contentions, I reserve the right to respond.

C. "writing control section" ('615 patent claim 11)

Solas's Proposed Construction	HP's Proposed Construction
Plain and ordinary meaning, i.e., circuit section that controls writing	a transistor that controls the writing of both the gradation sequence signal and the precharge voltage from a data line to the charge accumulating section

120. Claim 11 recites: "a plurality of display pixels each of which includes a light emission element and a light emission drive circuit having" having four recited "sections":

- "an electric charge accumulating section for accumulating electric charges based on a gradation sequence signal to designate a luminance gradation sequence in accordance with display data,"
- "a light emission control section for generating a light emission drive current having a predetermined current value in accordance with the electric charges accumulated in the electric charge accumulating section and supplying the light emission drive current to the light emission element, "
- "a writing control section for controlling a supplying state of the electric charges based on the gradation sequence signal to the electric charge accumulating section," and
- "a voltage control section for controlling a drive voltage for making the light emission control section perform the operation,"

121. Each of these recited sections refer back to the "light emission drive circuit"—they are sections of the drive circuit. That is the plain meaning of writing control section, and is used the

patent in accordance with that plain meaning, i.e., circuit section that controls writing. That is consistent with the claims and specification. For example, the claim describes "a writing control section" as performing the function of "controlling a supplying state of the electric charges based on the gradation sequence signal to the electric charge accumulating section." Claim 11.

122. Based on the specification, a POSITA would understand that the writing control section is a circuit section that controls writing, and may comprise circuitry such as transistor. *See* '615 patent at Fig. 1 and related description at column 17. This comports well with the Solas proposed construction and would be easily understood by a POSITA.

123. HP's proposal is "a transistor that controls the writing of both the gradation sequence signal and the precharge voltage from a data line to the charge accumulating section." HP's proposal is confusing and unsupported. It is not the plain meaning of "writing control section" nor required by the specification or claims. For example, the writing control section is not limited a single transistor as HP may imply or a single transistor that necessarily "controls the writing of ***both*** the gradation sequence signal and the precharge voltage from a data line to the charge accumulating section. I have reviewed the specification and prosecution history and do not see any redefinition of writing control section to mean HP's proposal or any disclaimer that would support it.

D. "data lines" ('615 patent claim 11)

Solas's Proposed Construction	HP's Proposed Construction
Plain and ordinary meaning, i.e., conductive lines for supplying information	conductive lines, each connected to and carrying data to a plurality of light emission drive circuits

124. The term "data line" is used eighty eight times throughout the '615 patent in a consistent and clear manner. Data line is a well-known term in the art. The term "data line" is readily understood by a POSITA, has a plain and ordinary meaning, and is used in the '615 patent in

accordance with that plain meaning, i.e., conductive lines for supplying information. For example, McGraw-Hill Dict. provides the following definition: "data transmission line: [ELEC] A system of electrical conductors, such as a coaxial cable or pair of wires, used to send information from one place to another or one part of a system to another." For example, the patent teaches that gradation sequence signals and a precharge voltage can be applied to the data lines. *See* '615 patent at 5:49–50 ("a data driver ….supplies a gradation sequence signal to the data line"); *see also* Fig. 1 and 17:5–16 (describing DL in Fig. 1 as a data line). This is consistent with Solas's proposal, which is that data lines are conductive lines for supplying information.

125. HP's proposal is incorrect and unsupported and not the plain and ordinary meaning. For example, the specification does not state that each individual data line must be connected to and carrying data to a plurality of light emission drive circuits. HP's proposal purports to require a one to many relationship between data lines and a light emission drive circuit. But this requirement is not part of the plain meaning of "data lines" or required by the intrinsic evidence. I have reviewed the specification and file history and found no lexicography or disclaimer to support HP's construction. Finally, HP purports to repeat the word "data" in the construction, so its construction is unhelpful and does not offer any additional clarification. The Court may as well find that "data lines" carries its plain and ordinary meaning and no further construction is required.

XI. CONCLUSION

I declare under penalty of perjury that the foregoing is true and correct.

Executed June 25, 2020, in San Ramon, California.

By: _____
Richard A. Flasck